REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

1. Amendments to Claims and Specification

Claim 1 has been amended by adopting the changes to line 7 of claim 1 suggested in item 1 on page 2 of the Official Action, by changing "second comparison voltage" to the more descriptive phrase –reference detection voltage–, and by positively reciting adjustment of the resistance ratio of the resistor pair, the resistance of the reference resistor, and an area ratio of the transistor pair for the purpose of reducing temperature coefficient impact. The specification has been amended to provide clear antecedent basis for the range recitation.

It is respectfully submitted that the more positive recitation of the adjustments that affect the temperature coefficient in claim 1 does not introduce **new matter** since the recited adjustments are explicitly supported by, for example, page 5, line 19 to page 6, line 5 of the original specification, which state that:

> *As cited, adjusting ratio for the resistor 32 to resistor pair 31, 32 and area ratio of the BJT pair 34, 35 can eliminate the temperature coefficients of the bandgap reference voltage completely. Similarly, in this embodiment, adjusting resistance ratio for the reference resistor 42 to resistor pair 411, 412 (i.e., adjusting the value of references resistor 42) and area ratio for the transistor pair 43 can eliminate temperature effect completely.*

This passage clearly supports the corresponding additions to claim 1.

2. Rejection of Claims 3 and 4 Under 35 USC §112, 2nd Paragraph

This rejection has been addressed by amending claim 3 to include the formula (previously omitted due to a quirk in the word processing program used to type the claims), and by clarifying that the ratio does not always apply.

Claim 4 has been canceled.

3. Rejection of Claims 1-4 and 6 Under 35 USC §103(a) in view of U.S. Patent Nos. 5,814,995 (Tasdighi) and 5,521,489 (Fukami)

This rejection is respectfully traversed on the grounds that the Examiner has misinterpreted the Tasdighi and Fukami patents in the following manner:

a. The alleged "voltage detector" of the Tasdighi patent is not connected to, and does not detect, the input voltage; and

b. The cascoded transistors of Fukami are not used to match a reference voltage with a change in the input voltage, but rather simply increases the input voltage.

As a result of these differences, described in more detail below, the proposed combination of the Tasdighi and Fukami patents could not possibly have resulted in the claimed invention.

According to the Examiner, Figure 7 of the Tasdighi reference discloses a voltage detector circuit which includes a resistor pair (R2, R3) connected to an input voltage; a reference resistor (R1) connected to one resistor (R2) of the resistor pair (R2, R3) for producing a first comparison voltage; at least one transistor pair (65, 66) connected to the other resistor (R3) of the resistor pair (R2, R3) and the reference resistor (R1) for producing a second comparison voltage; and a comparator (56) for comparing the first comparison voltage and the second comparison voltage for outputting a voltage level (Vout). In particular, the Examiner deems this voltage detector circuit to be similar to the claimed voltage detector of the present application. This is a misinterpretation of the Tasdighi patent.

The reason that the voltage detector described by the Examiner does not correspond to the claimed voltage detector is that the transistor pair (R2, R3) of the Tasdighi patent is not connected to the input voltage (Vin). Instead, as shown in Figure 7 of the Tasdighi patent, the transistor pair (R2, R3) is connected to a resistor divider formed of resistors RD and RU. It is known that the resistors RD and RU are employed to partition the input voltage, and thus the resistors RD and RU may function similar to the resistor 412 (R2) and resistor 42 (R3) of the present application. On the other hand, neither of the resistors R2 and R3 of Tasdighi is used to partition the input voltage. As a result, it is clear that the transistor pair (R2, R3) of the Tasdighi

reference is different from the resistor pair 41 (R1, R2) of the present application, both with respect to their connections and their function, and that the voltage detector circuit of the Tasdighi patent does not correspond to the claimed voltage detector.

In the sentence bridging pages 4 and 5 of the Official Action, the Examiner indicates that Figure 4 of the Fukami reference discloses a plurality of cascoded transistor pairs (42-42) in which the first comparison voltage (Va), the second comparison voltage (Vb), the difference of the first and second comparison voltage (Va, Vb) and the output voltage (Vout) depend on the plurality of cascoded transistor pairs. Again, the Examiner has misinterpreted the reference.

The reason that the cascoded transistor pairs of Fukami do not correspond to the claimed pairs is that **the cascoded transistor pairs of Fukami are not used to detect any voltage**. Instead, Figure 4 of the Fukami reference is a bandgap voltage source (BGR circuit 35) and not a voltage detector, and this bandgap voltage source 35 is used in an overheat detection circuit (see Figure 3 of the Fukami reference) to provide an output voltage VR which is constant independently from the fluctuation of the power source voltage and temperature variation (column 1, lines 26-35). In contrast, the cascoded transistor pairs of the present application are used in a voltage detector to provide a larger reference detection voltage, such as $2V_{BG}$, $3V_{BG}$, $4V_{BG}$,..., so that a larger input voltage still can be detected. Specifically, when the input voltage becomes twice, three times, or even four times, the number of cascoded transistor pairs is designed to be two, three, or four to provide twice, three times, or four times of reference detection voltage, so that the resistance ratio of the resistor pair 41, the resistance of the reference resistor 42 and the area ratios of the transistor pairs can be adjusted to reduce temperature coefficient impact. Although it may be known to those skilled in the circuit design that cascoded transistor pairs can increase (by twice, three times, four times,...) the provided reference voltage, the present application applies this reference voltage to match with the change of the input voltage, which is fundamentally different from the Fukami patent, which merely applies the reference voltage to provide a higher output voltage.

As a result of these differences, the applicant respectfully submits that proposed combination of the Tasdighi and Fukami patents, considered in any reasonable combination, would not have resulted in the claimed invention, and withdrawal of the rejection of claims 1-4 and 6 under 35 USC §103(a) is respectfully requested.

4. Rejection of Claim 7 Under 35 USC §103(a) in view of U.S. Patent Nos. 5,814,995 (Tasdighi), 5,521,489 (Fukami), and 5,731,686 (Malhi)

This rejection is respectfully traversed on the grounds that the Malhi patent, like the Tasdighi and Fukami patents, fails to disclose or suggest a comparator having a detection voltage level and at least one transistor pair having a cascoded number that varies with the detection voltage level as claimed in claim 1.

Instead, as noted in the previous response, the Malhi patent discloses over-temperature protection for a battery regulator that lacks any sort of cascoded transistor pairs. Furthermore, Malhi fails to even disclose the claimed power disconnection switch coupled between a resistor pair and the input voltage, since MOSFET switch Q1 of Malhi is actually controlled to provide a constant battery output voltage rather than power-saving power disconnection. As a result, the Malhi patent cannot make up for the deficiencies of the Tasdighi and Fukami patents, and withdrawal of the rejection of claims 7 under 35 USC §103(a) is respectfully requested.

Having thus overcome each of the rejections made in the Official Action, withdrawal of the rejections and expedited passage of the application to issue is requested.

Respectfully submitted,

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